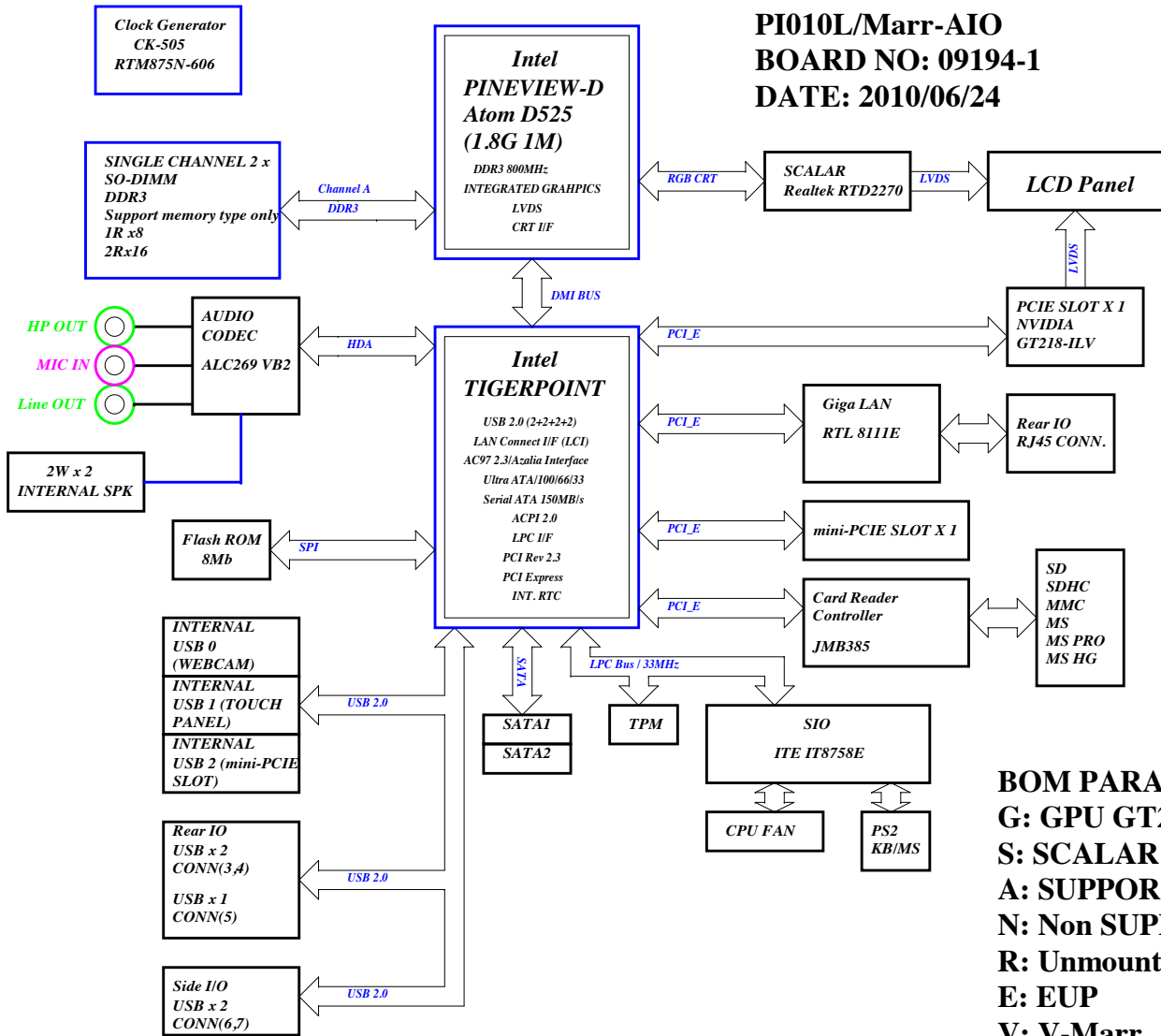


E/VMARR_Pine trail-D Block Diagram



PI010L/Marr-AIO
BOARD NO: 09194-1
DATE: 2010/06/24

PAGE	TITLE	Quantity
01	COVER PAGE	
02	POWER DELIVERY CHART	
03	CLOCK/RESET MAP	
04	POWER MAP	
05	GPIO TABLE	
06	CLOCK GENERATOR	
07	CPU PINEVIEW:DMI&EXP/ VGA/VSS	
08	CPU PINEVIEW:DDR3	
09	CPU PINEVIEW:LVDS/CPU SB/DEBUG	
10	CPU PINEVIEW:POWER	
11	DDR3 DIMMA & B	
12	DDR3 DECOUPLING	
13	LVDS RTD2270	
14	GPU NV GT218-ILV	
15	TP DMI/ PCIE/ USB	
16	TP HOST/ SATA	
17	TP GPIO/ SPI/ LPC/ RTC	
18	TP POWER/ GND	
19	USB CONNECTOR	
20	LAN RTL8111E	
21	AUDIO CODEC ALC269	
22	SATA/ XPD-SSA/DEBUG PORT	
23	SIO ITE8758/FAN/PS2 KBMS	
24	MINI-PCIE SLOT	
25	CARD READER JMB385C	
26	19VDC POWER JACK	
27	S5 1W/ LED/ HOLES	
28	RT8205A 3V&5V	
29	RT8209A DDR1D5V/1D05V	
30	RT8209A GPU CORE	
31	NCP5380_VCORE	
Total:		

BOM PARAMETER

G: GPU GT218-ILV
S: SCALAR RTD2270
A: SUPPORT ASF 2.0
N: Non SUPPORT ASF 2.0
R: Unmount
E: EUP
V: V-Marr
D: D-SUB

EMARR_H: G, N
EMARR_L: S, N
VMARR: S, A, V

POWER ADAPTER
ADP_19V

VCORE
+1.1V NCP5380 (8A)

Phase 1
NTD4809N NMOS
TO-252 14m ohm
VCORE
NTD4806N NMOS
TO-252 9.4m ohm

5V S5
RT8205A
AO4468 NMOS
SO-8 22m ohm
5V_S5
AO4718 NMOS
SO-8 14m ohm
3D3V S5
AO4468 NMOS
SO-8 22m ohm
3D3V_S5
AO4718 NMOS
SO-8 14m ohm

VCC5 (6.5A)
AO4468
NMOS SO-8
14mohm 9.2A
5V_S0
SLP_S3_N

VCC5
AO4468
NMOS SO-8
14mohm 9.2A
5V_S5
SLP_S4_N
VCC5_USB

VCC3_3 (4A)
AO4468
NMOS SO-8
14mohm 9.2A
3D3V_S5
SLP_S3_N
3D3V_S0

MEMORY POWER (18A)
+1.8V RT8209A
ADP_19V
NTD4809N NMOS
TO-252 14m ohm
VCC_MEM_1P5
5V_S5
NTD4806N NMOS
TO-252 9.4m ohm

+0.9V (1A)
APL5336
LDO SO-8 1.5A
MEM_VTT

CORE POWER
+1.5V
AO4468
NMOS SO-8
14mohm 9.2A
OP

(2.5A)
NM10
V_1P5_CORE

GT218 CORE POWER
0.9V RT8209A
ADP_19V
NTD4809N NMOS
TO-252 14m ohm
VCC_MEM_1P5
5V_S5
NTD4806N NMOS
TO-252 9.4m ohm

(11.3A)
GPU GT218-ILV
V_OP9_CORE

AO4468
NMOS SO-8
14mohm 9.2A

(2A)
GPU GT218-ILV
V_1P5_MEM

+1.05V
AO4468
NMOS SO-8
14mohm 9.2A
OP

V_1P05_CORE

(6.5A)
NM10
V_1P05_CORE

(0.72A)
GPU GT218-ILV
V_1P05

5V_S0
CPU Fan
WEBCAM
Touch Panel (Option)
3D3V_S0
SIO ITE8755
LAN RTL8111E
CLK GEN
RTM875N-605
BIOS ROM
1394/Card reader
VT6325
LVDS RTL2270
AUDIO ALC269

CPU	
VCORE	VCORE +1.1V 8A
V_1P05_CORE	V_1P05_CORE 5.34A
VCCA	VCCA 1.5V 0.11A
V_SM	V_SM 2.27A
V_1P8_PLLSFR	V_1P8_PLLSFR 0.43A
VCC_GIO	VCC_GIO 0.01A

SB	
Vcc1.05V	Vcc1.05V 0.98A
Vcc1_5_V	Vcc1_5_V 1.41A
VCC3_3	VCC3_3 0.29A
V5REF	V5REF 0.006A
VCCSus3_3	VCCSus3_3 0.13A
V5REF_Sus	V5REF_Sus 0.01A
VccRTC	VccRTC 0.014A

DDR2 2 DIMM	
VCC_MEM_1P5	V_SM 1.0A
MEM_VTT	V_SM_VTT 0.3A

Mini PCI Express Slot x 1	
3D3V_S0	V_SM 1.0A
V_1P5_CORE	V_SM_VTT 0.3A

Vinafix

CK 505

3.3 VOLT

CK_PWRGD

PCI

PCIF5

PCI0

USB

UCB48

REF

REF

SRC

SRC2

SRC2*

SRC3

SRC3*

SRC5

SRC5*

SRC7

SRC7*

SRC6

SRC6*

SRC0

SRC0*

SRC1

SRC1*

SRC4

SRC4*

HOST

CPU0*

CPU0

CPU1*

CPU1

CPU_ITP*

CPU_ITP

CRYSTAL

32.768KHZ

32.768KHZ

RTCX1
RTCX2
PCICLK

SMBCLK
ACZ_BCLK

24MHZ

SCLK

AUDIO CODEC

BCLK

GLUE LOGIC

ICH_RSMRST_N

PWRGD_3V

TIGERTPOINT

PLTRSTB

RSMRST#

CPUPWRGOOD

VRMPWRGD

DMICLK100N

DMICLK100P

SATACLKN

SATACLKP

PLTRST_N

VCC3

LRESET#

RSMRST#

PCICLK

CLKIN

PWROK

PWRGD_3V

PWROK

CLK48

CLK14

PCICLK

CLKIN

PWROK

PWRGD_3V

PWROK

CLK48

CLK14

PCICLK

CLKIN

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PCICLK

CLKIN

PWROK

PWRGD_3V

PWROK

CLK48

CLK14

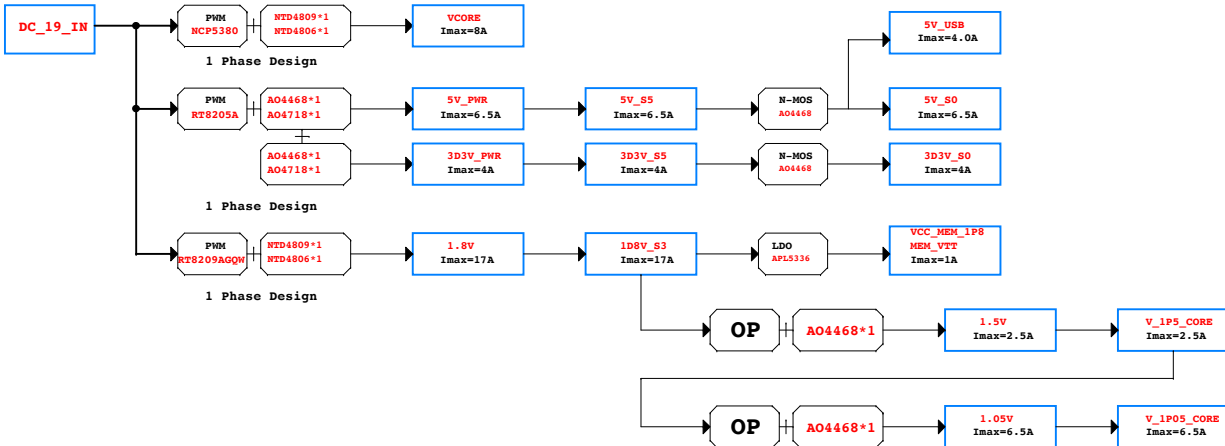
PCICLK

CLKIN

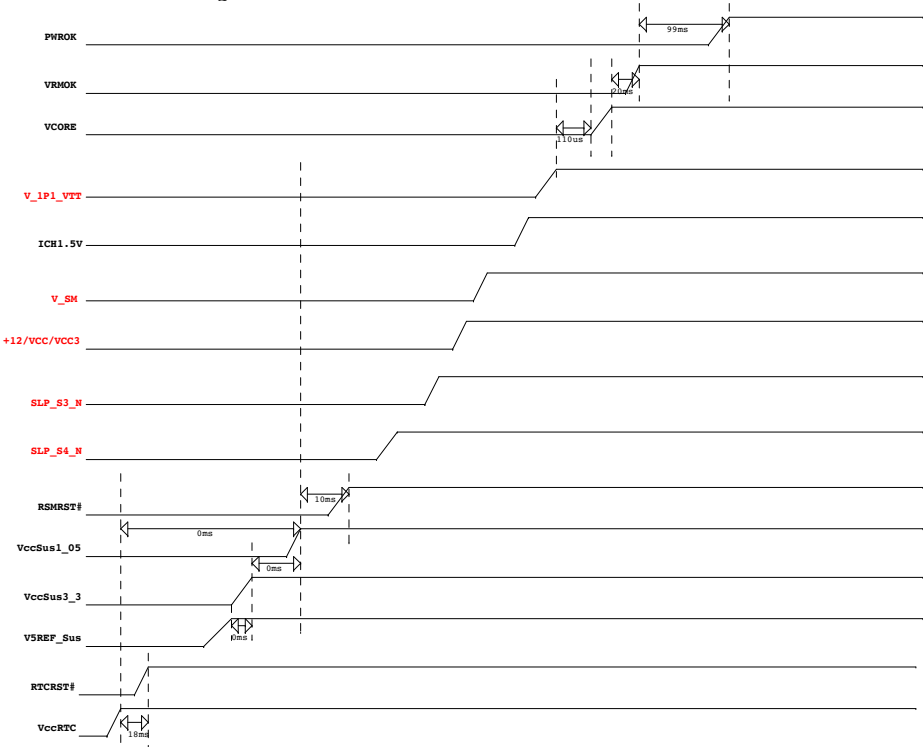
PWROK

PWRGD_3V

CPU POWER CONN




POWER ON SEQUENCE



PCH TIGERPOINT

S5 -> LAN_PWR_ON -> LOW
S4, S3, S0 -> LAN_PWR_ON -> HIGH

PIN NAME	PIN#	POWER WELL	USAGE	Default Type	DURING RESET	Default Setting	NOTES
GPIO0	T15	MAIN	PANEL_DET	I/O		H	Multiplexed with BM_BUSY#.
GPIO1	C9	MAIN	SPK_MUTE_N	I/O		H	Unmultiplexed.
GPIO2	E8	MAIN	P_INTE_N	I/OD		H	Multiplexed with PIRQ[H:E]#.
GPIO3	D6	MAIN	P_INTF_N	I/OD		H	Multiplexed with PIRQ[H:E]#.
GPIO4	H8	MAIN	P_INTG_N	I/OD		H	Multiplexed with PIRQ[H:E]#.
GPIO5	F8	MAIN	P_INTH_N	I/OD		H	Multiplexed with PIRQ[H:E]#.
GPIO6	W16	MAIN	W1_DETECT_N	I/O		H	Unmultiplexed.
GPIO7	W14	MAIN	W2_DETECT_N	I/O		H	Unmultiplexed.
GPIO8	K18	RESUME	PANEL_SEL1	I/O		H	Unmultiplexed.
GPIO9	H19	RESUME	PANEL_SEL2	I/O		H	Unmultiplexed.
GPIO10	M17	RESUME	PANEL_SEL3	I/O		H	Unmultiplexed.
GPIO11	E20	RESUME	SMB_ALERT_PU	I/O		H	Multiplexed with SMBALERT#
GPIO12	A24	RESUME	P_GPIO12	I/O		H	Unmultiplexed.
GPIO13	C23	RESUME	PME_N	I/O		H	Unmultiplexed.
GPIO14	P5	RESUME	TS_RADY	I/O		H	Unmultiplexed. 7/9
GPIO15	E24	RESUME	P_GPIO15	I/O		L	Unmultiplexed.
GPIO16		N/A		N/A			Not Implemented
GPIO17	A2	MAIN	P_GPIO17	I/O		L	Multiplexed with BM_BUSY#.
GPIO18		N/A		N/A			Not Implemented
GPIO19		N/A		N/A			Not Implemented
GPIO20		N/A		N/A			Not Implemented
GPIO21		N/A		N/A			Not Implemented
GPIO22	C15	MAIN	Panel_FB	I/O		H	Unmultiplexed.
GPIO23	AA5	MAIN	L_DRQ1_N	I/O			Multiplexed with LDRQ1#
GPIO24	R3	RESUME	LAN_PWR_ON	I/O		H	Unmultiplexed. Not cleared by CF9h reset event.
GPIO25	C24	RESUME	TPEV_P_GPIO25	I/O		L	Unmultiplexed.
GPIO26	D19	RESUME	ISPWT_EN_R	I/O		H	Unmultiplexed.
GPIO27	D20	RESUME	SUSLED_N	I/O		H	Unmultiplexed.
GPIO28	F22	RESUME	PWRLED_N	I/O		H	Unmultiplexed.
GPIO29	E6	RESUME	-USB_OC57	I/O		H	Multiplexed with OC5#
GPIO30	C2	RESUME	-USB_OC36	I/O		H	Multiplexed with OC6#
GPIO31	C3	RESUME	-USB_OC57	I/O		H	Multiplexed with OC7#
GPIO32		N/A		N/A			Not Implemented
GPIO33	U14	MAIN	W1_DISABLE_N	I/O			Unmultiplexed.
GPIO34	AC1	MAIN	W2_DISABLE_N	I/O			Unmultiplexed.
GPIO35		N/A		N/A			Not Implemented
GPIO36	AD23	MAIN	AUTO_COLOR_SIO	I/O			Unmultiplexed.
GPIO37		N/A		N/A			Not Implemented
GPIO38	AC23	MAIN	TOUCH_EN	I/O		H	Unmultiplexed.
GPIO39	AC24	MAIN	CAMERA_EN	I/O		H	Unmultiplexed.
GPIO40		N/A		N/A			Not Implemented.
GPIO41		N/A		N/A			Not Implemented.
GPIO42		N/A		N/A			Not Implemented.
GPIO43		N/A		N/A			Not Implemented.
GPIO44		N/A		N/A			Not Implemented.
GPIO45		N/A		N/A			Not Implemented.
GPIO46		N/A		N/A			Not Implemented.
GPIO47		N/A		N/A			Not Implemented.
GPIO48	G14	MAIN	P_GPIO48	I/O		L	Multiplexed with STRAP1#
GPIO49	AB22	CPU	H_PWRGD	I/O		H	Multiplexed with CPUPWRGD

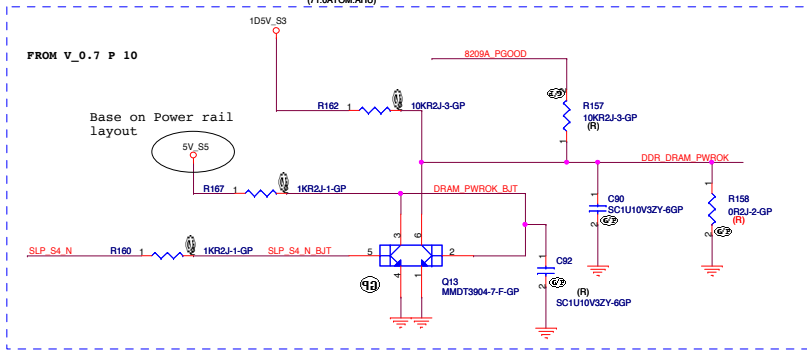
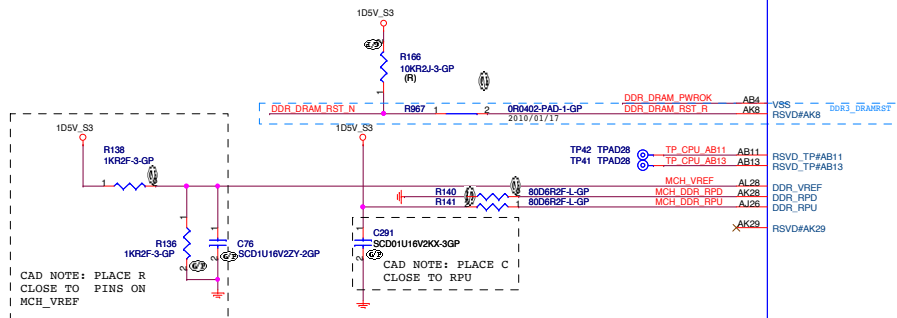
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Title GPIO TABLE			
Size A3	Document Number AIO eMARR		Rev 1A
Date:	Thursday, June 24, 2010	Sheet	5 of 31

DIMM

11 M_MAA_A[14..0]	M_MAA_A[14..0]
11 M_SBS_A2	M_SBS_A2
11 M_SBS_A1	M_SBS_A1
11 M_SBS_A0	M_SBS_A0
11 M_SCS_A_N3	M_SCS_A_N3
11 M_SCS_A_N2	M_SCS_A_N2
11 M_SCS_A_N1	M_SCS_A_N1
11 M_SCS_A_N0	M_SCS_A_N0
11 M_SCKE_A3	M_SCKE_A3
11 M_SCKE_A2	M_SCKE_A2
11 M_SCKE_A1	M_SCKE_A1
11 M_SCKE_A0	M_SCKE_A0
11 M_ODT_A3	M_ODT_A3
11 M_ODT_A2	M_ODT_A2
11 M_ODT_A1	M_ODT_A1
11 M_ODT_A0	M_ODT_A0
11 M_DATA_A[63..0]	M_DATA_A[63..0]
11 M_WE_A_N	M_WE_A_N
11 M_CAS_A_N	M_CAS_A_N
11 M_RAS_A_N	M_RAS_A_N
11 CK_M_DDR0_A_DP	CK_M_DDR0_A_DP
11 CK_M_DDR0_A_DN	CK_M_DDR0_A_DN
11 CK_M_DDR1_A_DP	CK_M_DDR1_A_DP
11 CK_M_DDR1_A_DN	CK_M_DDR1_A_DN
11 CK_M_DDR3_A_DP	CK_M_DDR3_A_DP
11 CK_M_DDR3_A_DN	CK_M_DDR3_A_DN
11 CK_M_DDR4_A_DP	CK_M_DDR4_A_DP
11 CK_M_DDR4_A_DN	CK_M_DDR4_A_DN
11 M_DQS_A_DP0	M_DQS_A_DP0
11 M_DQS_A_DP1	M_DQS_A_DP1
11 M_DQS_A_DP2	M_DQS_A_DP2
11 M_DQS_A_DP3	M_DQS_A_DP3
11 M_DQS_A_DP4	M_DQS_A_DP4
11 M_DQS_A_DP5	M_DQS_A_DP5
11 M_DQS_A_DP6	M_DQS_A_DP6
11 M_DQS_A_DP7	M_DQS_A_DP7
11 M_DQS_A_DN0	M_DQS_A_DN0
11 M_DQS_A_DN1	M_DQS_A_DN1
11 M_DQS_A_DN2	M_DQS_A_DN2
11 M_DQS_A_DN3	M_DQS_A_DN3
11 M_DQS_A_DN4	M_DQS_A_DN4
11 M_DQS_A_DN5	M_DQS_A_DN5
11 M_DQS_A_DN6	M_DQS_A_DN6
11 M_DQS_A_DN7	M_DQS_A_DN7
11 M_DOM_A0	M_DOM_A0
11 M_DOM_A1	M_DOM_A1
11 M_DOM_A2	M_DOM_A2
11 M_DOM_A3	M_DOM_A3
11 M_DOM_A4	M_DOM_A4
11 M_DOM_A5	M_DOM_A5
11 M_DOM_A6	M_DOM_A6
11 M_DOM_A7	M_DOM_A7
11 DDR_DRAM_RST_N	DDR_DRAM_RST_N

MISC

17,23,28,29 SLP_S4_N	SLP_S4_N
29 8209A_PG00D	8209A_PG00D



CLOCK

6 CK_H_CPU_DN << CK_H_CPU_DN
6 CK_H_CPU_DP << CK_H_CPU_DP

6/22

Frequency select

6 BSEL0 <<—————

6 BSEL1 <<—————

6 BSEL2 <<—————

TPT

16	H_THERMTRIP_N	<<	H_THERMTRIP_N
16	H_SMI_N	>>	H_SMI_N
16	H_A20M_N	>>	H_A20M_N
16	H_FERR_N	>>	H_FERR_N
16	H_INTR	>>	H_INTR
16	H_NMI	>>	H_NMI
16	H_IGNNE_N	>>	H_IGNNE_N
16	H_STPCLK_N	>>	H_STPCLK_N
17	PM DPRSTP_P_N	>>	PM DPRSTP_P_N
17	H_DPSLP_N	>>	H_DPSLP_N
17	H_INIT_N	>>	H_INIT_N

SIO

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23 CPU_THERMDA << CPU_THERMDA
23 CPU_THERMDC >> CPU_THERMDC

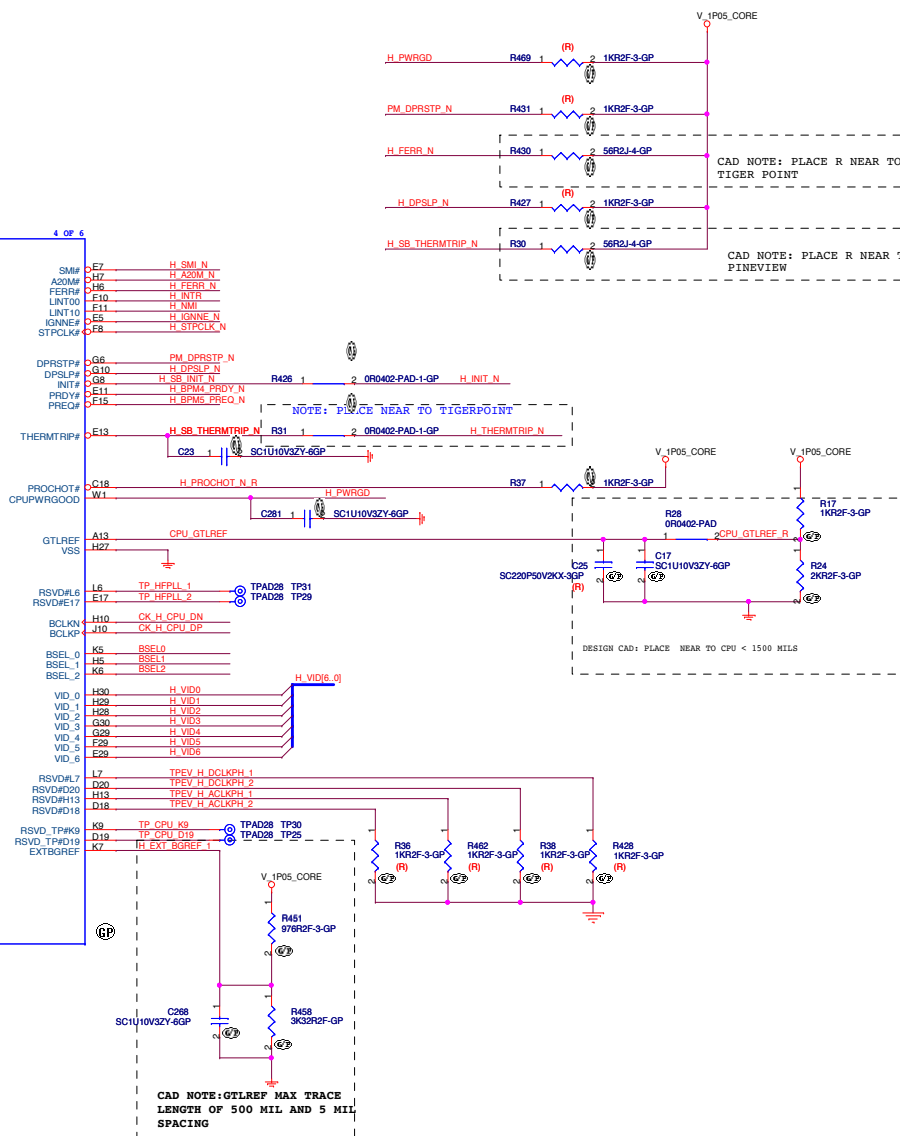
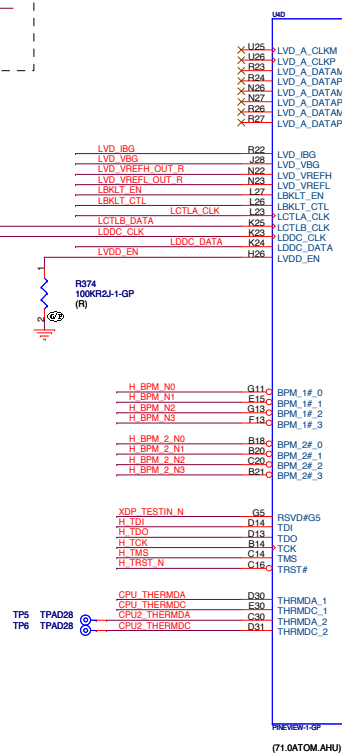
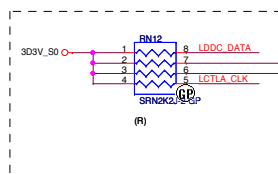
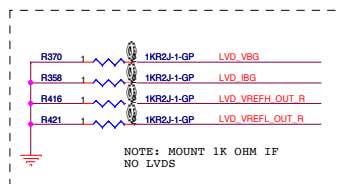
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XDP-SSA

17	H_PWRGD	≡	H_PWRGD
22	XDP_TESTIN_N	≡	XDP_TESTIN_N
22	H_TDI	≡	H_TDI
22	H_TDO	≡	H_TDO
22	H_TCK	≡	H_TCK
22	H_TMS	≡	H_TMS
22	H_TRST_N	≡	H_TRST_N
22	H_BPM1_PRODY_N	≡	H_BPM1_PRODY_N
22	H_BPM5_PREQ_N	≡	H_BPM5_PREQ_N
22	H_BPM1_N0	≡	H_BPM1_N0
22	H_BPM1_N1	≡	H_BPM1_N1
22	H_BPM1_N2	≡	H_BPM1_N2
22	H_BPM1_N3	≡	H_BPM1_N3
22	H_BPM1_N0	≡	H_BPM1_N0
22	H_BPM1_N1	≡	H_BPM1_N1
22	H_BPM1_N2	≡	H_BPM1_N2
22	H_BPM1_N3	≡	H_BPM1_N3

VCCP VREG CONTROLLER

31 H_VID[6..0]  H_VID[6..0]

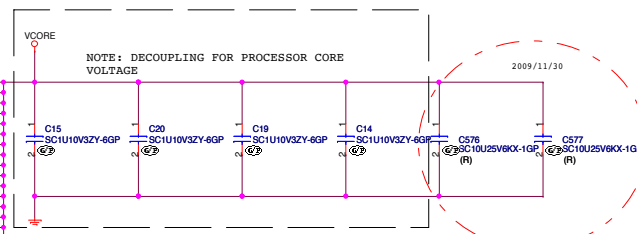
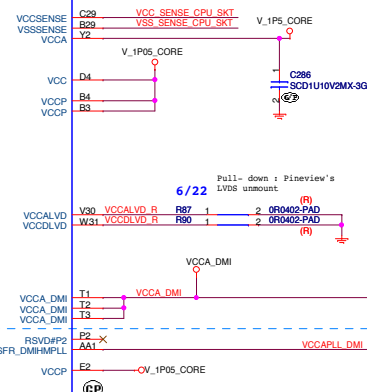
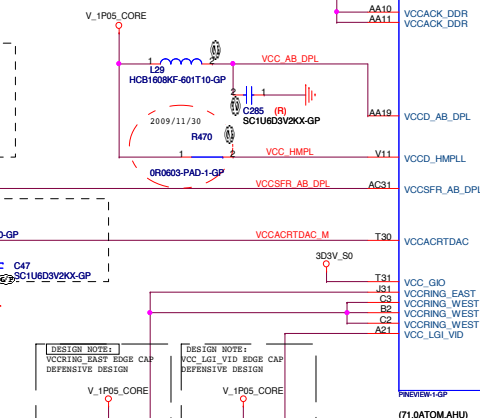
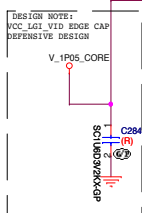
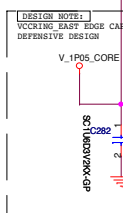
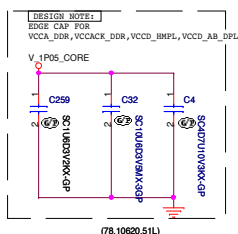
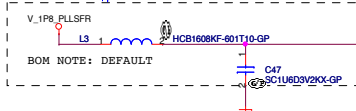
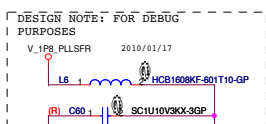
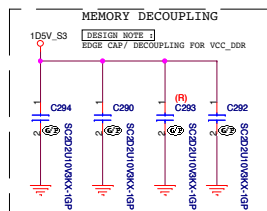
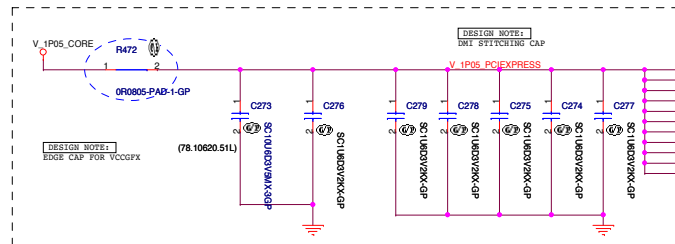


VCCP VERG CONTROLLER

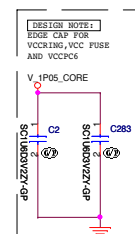
31 VCC_SENSE_CPU_SKT << VCC_SENSE_CPU_SKT
31 VSS_SENSE_CPU_SKT << VSS_SENSE_CPU_SKT

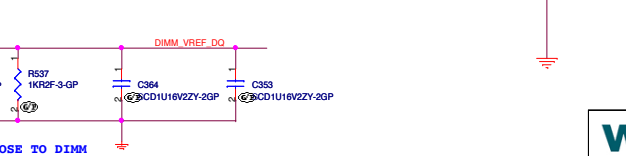
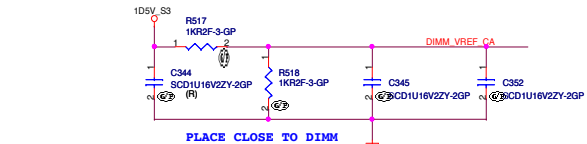
MISC

17,23,28,29,30 SLP_S3_N << SLP_S3_N



2009/11/20
VCCA_DMI (This circuit is defensive design for Pineview A0 only, you don't need it for currently B0 state)

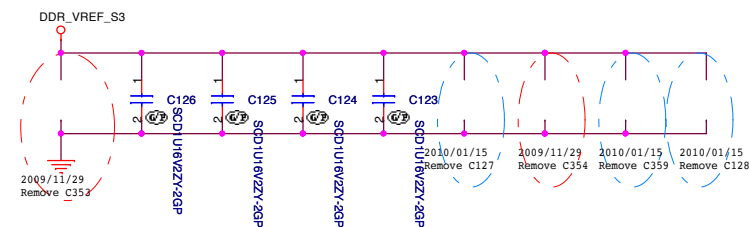




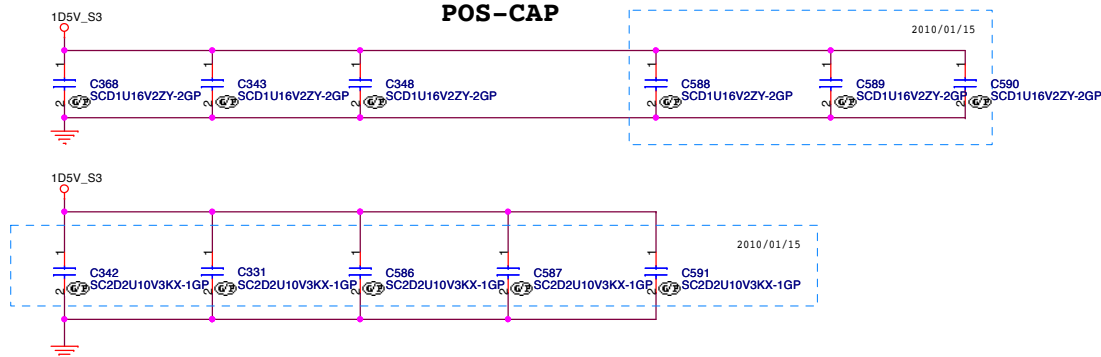
Stitching Caps place close to DIMM: Cross 1.8V and 0.9V

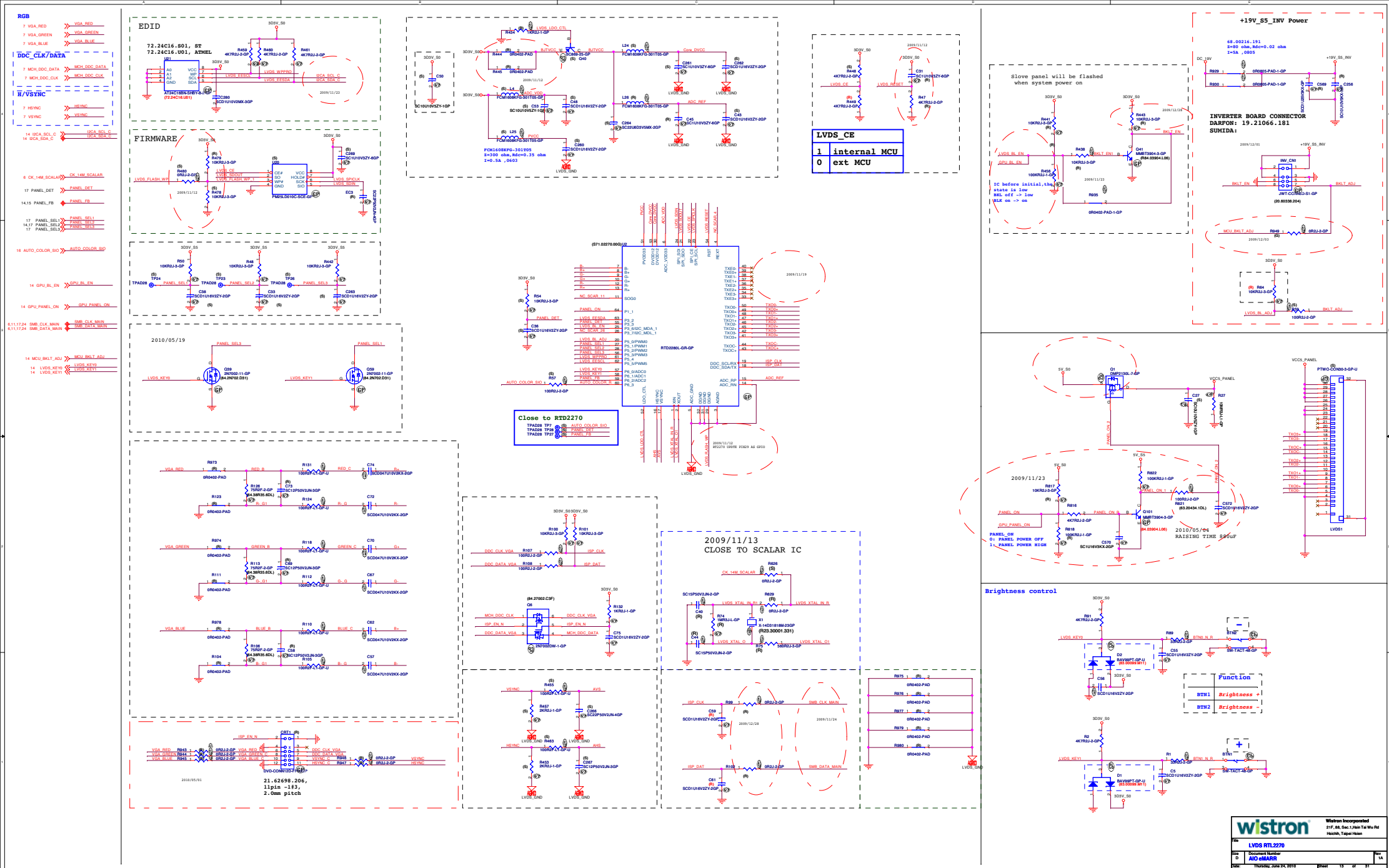
Don't Need.

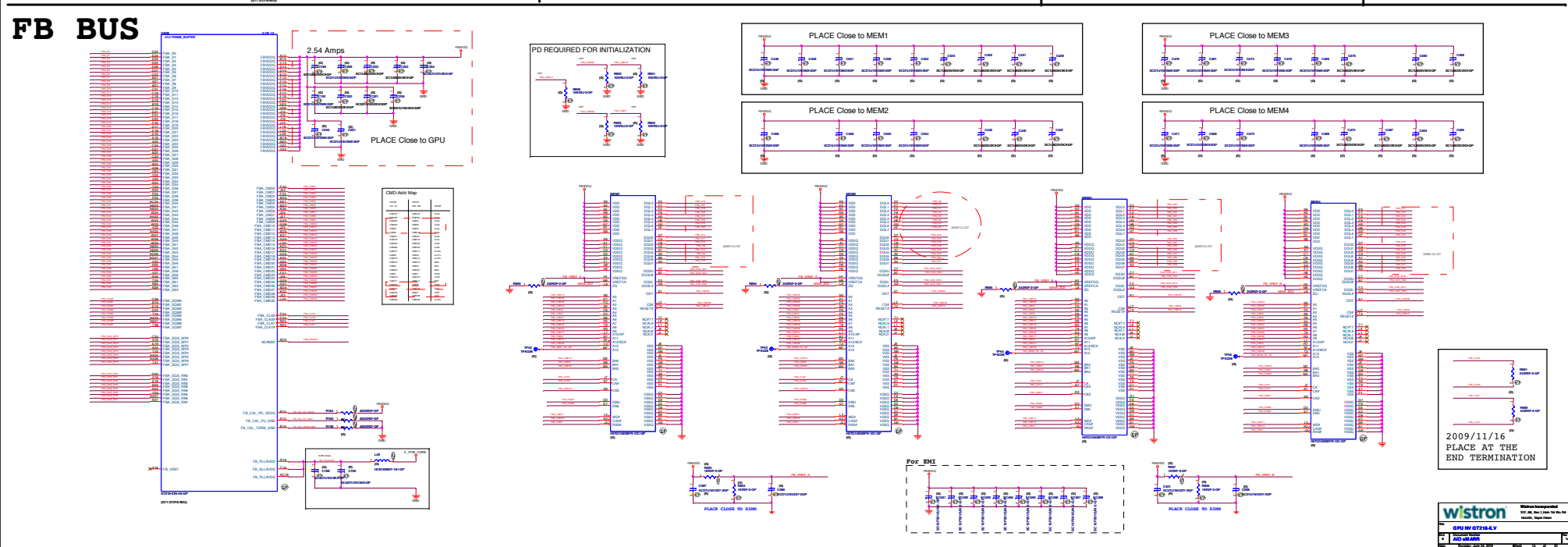
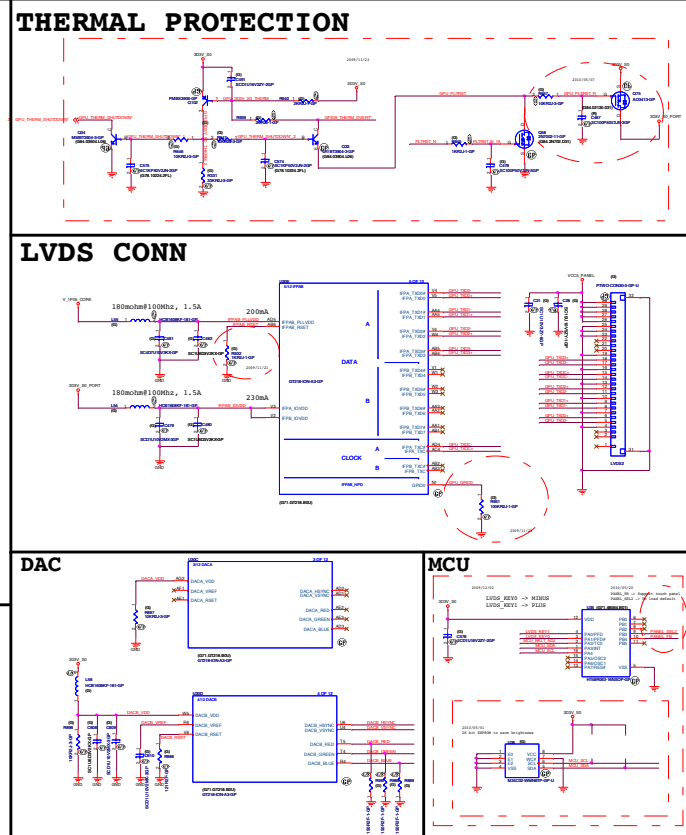
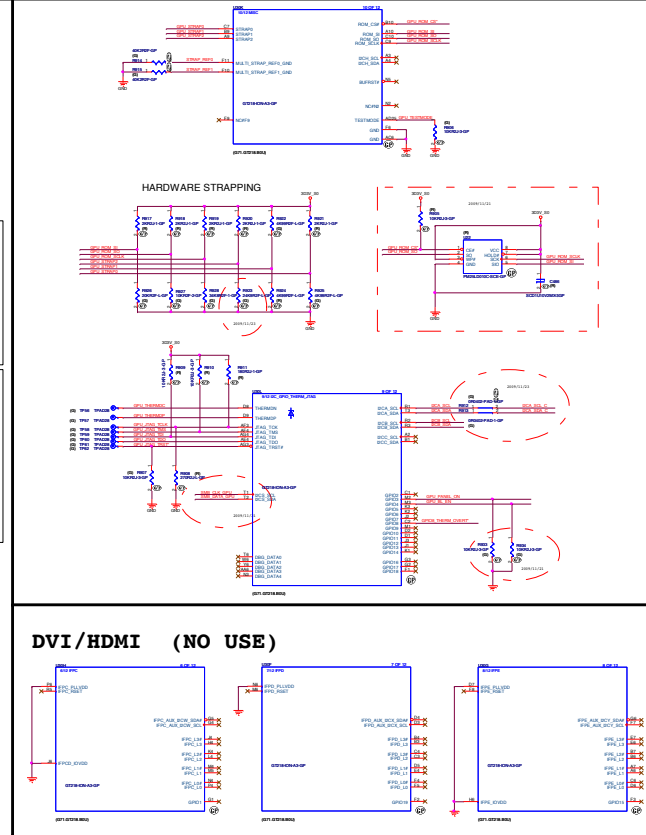
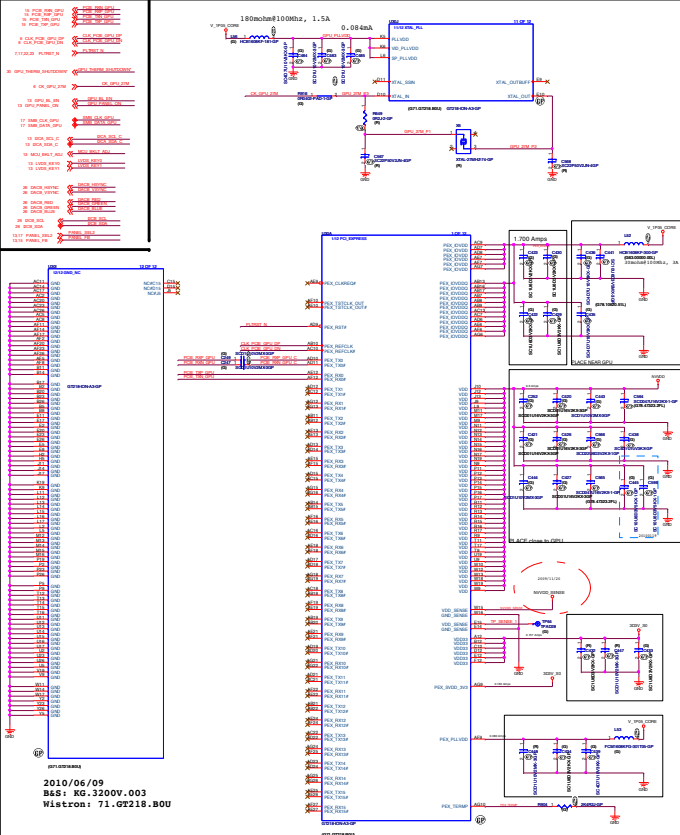
Channel A Decoupling Caps close to DIMM



POS-CAP







CLOCK

```

6 CK_P_33M_ICH >> CK_P_33M_ICH
6 CK_48M_USB_ICH >> CK_48M_USB_ICH
6 CK_PE_100M_ICH_DP >> CK_PE_100M_ICH_DP
6 CK_PE_100M_ICH_DN >> CK_PE_100M_ICH_DN

```

DMI

7 DMI_MCH_IT_MR_0_DP	DM1 MCH IT MR 0 DP
7 DMI_MCH_IT_MR_0_DN	DM1 MCH IT MR 0 DN
7 DMI_MCH_IT_MR_1_DP	DM1 MCH IT MR 1 DP
7 DMI_MCH_IT_MR_1_DN	DM1 MCH IT MR 1 DN
7 DMI_MCH_IT_MR_2_DP	DM1 MCH IT MR 2 DP
7 DMI_MCH_IT_MR_2_DN	DM1 MCH IT MR 2 DN
7 DMI_MCH_IT_MR_3_DP	DM1 MCH IT MR 3 DP
7 DMI_MCH_IT_MR_3_DN	DM1 MCH IT MR 3 DN

7	DMI_MCH_MT_IR_0_DP	7	DMI_MCH_MT_IR_0_DP
7	DMI_MCH_MT_IR_0_DN	7	DMI_MCH_MT_IR_0_DN
7	DMI_MCH_MT_IR_1_DP	7	DMI_MCH_MT_IR_1_DP
7	DMI_MCH_MT_IR_1_DN	7	DMI_MCH_MT_IR_1_DN
7	DMI_MCH_MT_IR_2_DP	7	DMI_MCH_MT_IR_2_DP
7	DMI_MCH_MT_IR_2_DN	7	DMI_MCH_MT_IR_2_DN
7	DMI_MCH_MT_IR_3_DP	7	DMI_MCH_MT_IR_3_DP
7	DMI_MCH_MT_IR_3_DN	7	DMI_MCH_MT_IR_3_DN

PCI-E

25	PCIE_RXN_CR	>>>	PCIE_RXN_CR
26	PCIE_RXP_CR	>>>	PCIE_RXP_CR
27	PCIE_TXN_CR	>>>	PCIE_TXN_CR
28	PCIE_TXP_CR	>>>	PCIE_TXP_CR
20	PCIE_RXN_LAN	>>>	PCIE_RXN_LAN
21	PCIE_RXP_LAN	>>>	PCIE_RXP_LAN
20	PCIE_TXN_LAN	>>>	PCIE_TXN_LAN
20	PCIE_TXP_LAN	>>>	PCIE_TXP_LAN
24	PCIE_RXN_MINI1	>>>	PCIE_RXN_MINI1
24	PCIE_RXP_MINI1	>>>	PCIE_RXP_MINI1
24	PCIE_TXN_MINI1	>>>	PCIE_TXN_MINI1
24	PCIE_TXP_MINI1	>>>	PCIE_TXP_MINI1
14	PCIE_RXN_GPU	>>>	PCIE_RXN_GPU
14	PCIE_RXP_GPU	>>>	PCIE_RXP_GPU
14	PCIE_TXN_GPU	>>>	PCIE_TXN_GPU
14	PCIE_TXP_GPU	>>>	PCIE_TXP_GPU

USB

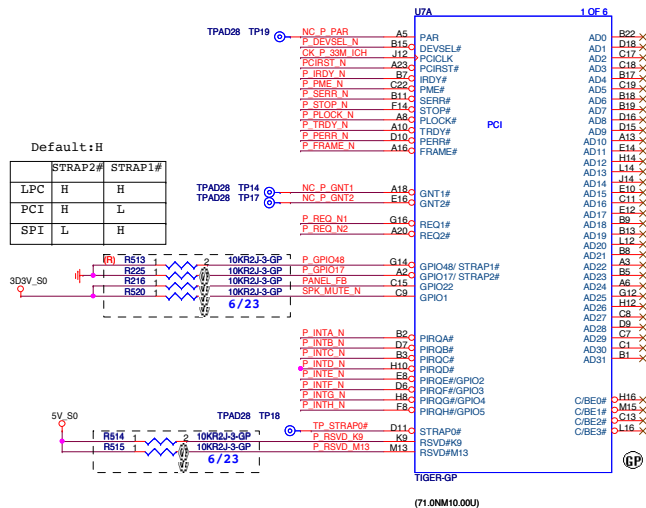
```

19 -USB_OC12      >> -USB_OC12
19 -USB_OC34s     >> -USB_OC34s

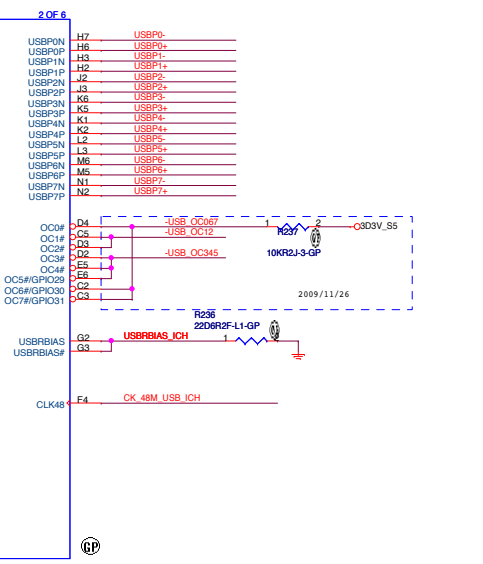
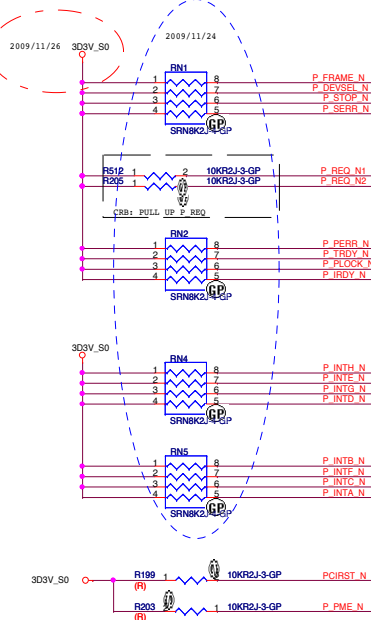
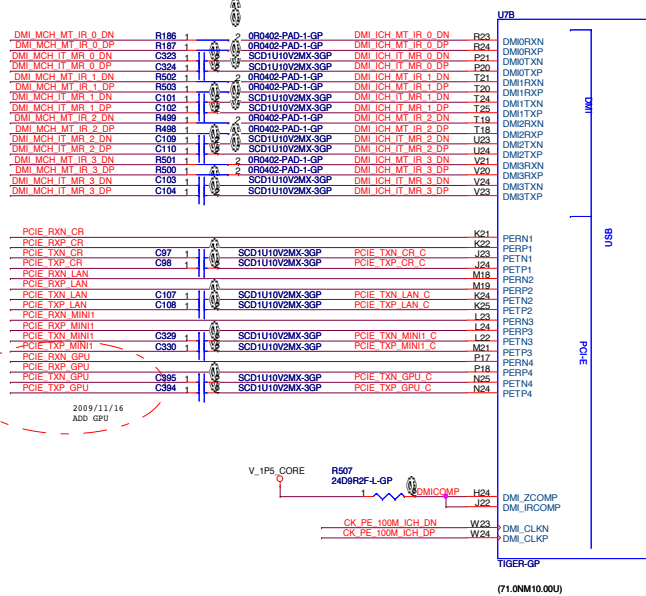
19 USBP0_         USBP0_
19 USBP0+         USBP0+
19 USBP1_         USBP1_
19 USBP1+         USBP1+
19 USBP2_         USBP2_
19 USBP2+         USBP2+
19 USBP3_         USBP3_
19 USBP3+         USBP3+
19 USBP4_         USBP4_
19 USBP4+         USBP4+
19 USBP5_         USBP5_
19 USBP5+         USBP5+
24 USBP6_         USBP6_
24 USBP6+         USBP6+
19 USBP7_         USBP7_
19 USBP7+         USBP7+

```

6/21
13.14 PANEL_FB  PANEL_FB



AC coupling caps need to be within 250 mils of the driver.



6 CK_IHSATA_DN >>> CK_IHSATA_DN
6 CK_IHSATA_DP >>> CK_IHSATA_DP

6 CK_ICHSAATA_DN >>> CK_ICHSAATA_DN
6 CK_ICHSAATA_DP >>> CK_ICHSAATA_DP

9 H_A20M_N	H_IGNNE_N
9 H_IGNNE_N	H_INIT_N
9 H_INIT_N	H_INTR
9 H_INTR	H_NMI
9 H_NMI	H_SMI_N
9 H_SMI_N	H_STPCLK_N
9 H_STPCLK_N	
17,22,23 SER_IRQ	SER_IRQ
9 H_FERR_N	H_FERR_N
9 H_THERMTRIP_N	H_THERMTRIP_N

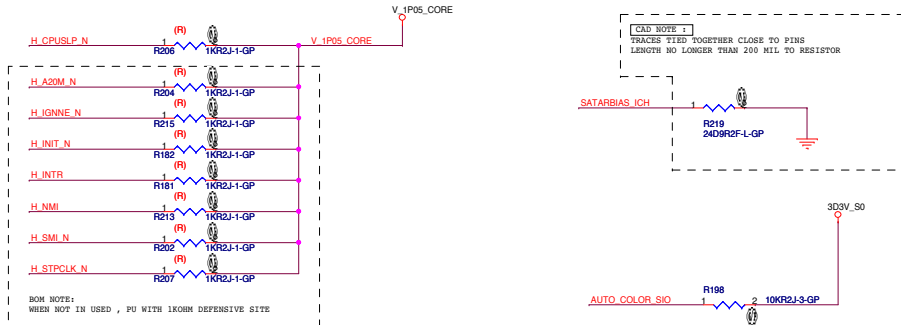
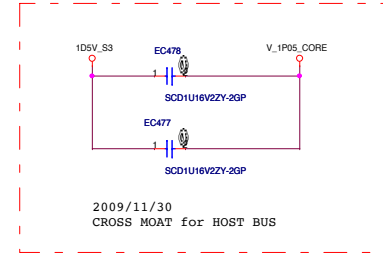
9	H_A20M_N	H_IGNNE_N
9	H_IGNNE_N	H_INIT_N
9	H_INIT_N	H_INTR
9	H_INTR	H_NMI
9	H_NMI	H_SMI_N
9	H_SMI_N	H_STPCLK_N
9	H_STPCLK_N	
17,22,23	SER_IRQ	SER_IRQ
9	H_FERR_N	H_FERR_N
9	H_THERMTRIP_N	H_THERMTRIP_N

22	SATAHDR_RX0_DP	SATAHDR_RX0_DP
22	SATAHDR_RX0_DN	SATAHDR_RX0_DN
22	SATAHDR_TX0_DP	SATAHDR_TX0_DP
22	SATAHDR_TX0_DN	SATAHDR_TX0_DN
22	SATAHDR_RX1_DP	SATAHDR_RX1_DP
22	SATAHDR_RX1_DN	SATAHDR_RX1_DN
22	SATAHDR_TX1_DP	SATAHDR_TX1_DP
22	SATAHDR_TX1_DN	SATAHDR_TX1_DN

22	SATAHDR_RX0_DN	SATAHDR_RX0_DP
22	SATAHDR_RX0_DP	SATAHDR_TX0_DN
22	SATAHDR_TX0_DN	SATAHDR_TX0_DP
22	SATAHDR_RX1_DN	SATAHDR_RX1_DP
22	SATAHDR_RX1_DP	SATAHDR_TX1_DN
22	SATAHDR_TX1_DN	SATAHDR_TX1_DP

23 KBRST_N >> KBRST_N

23 KBRST_N



CLOCK



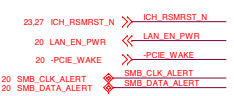
LPC



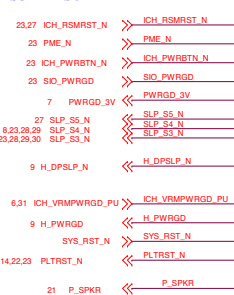
AUDIO



LAN



S5 -> S0



PNV



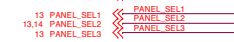
SMB



GPIO



13



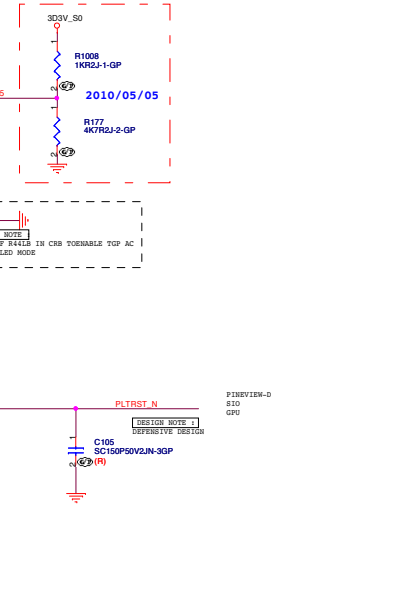
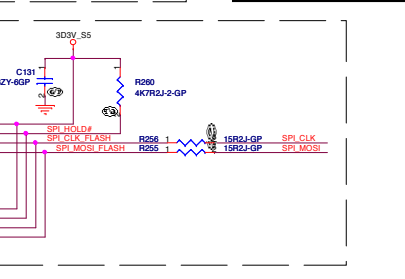
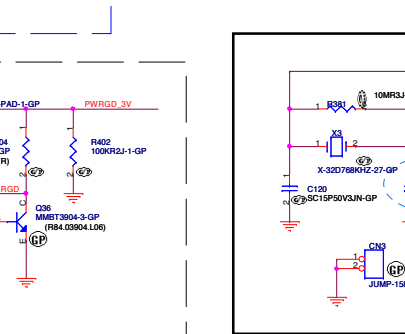
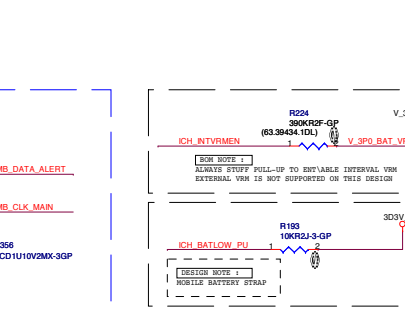
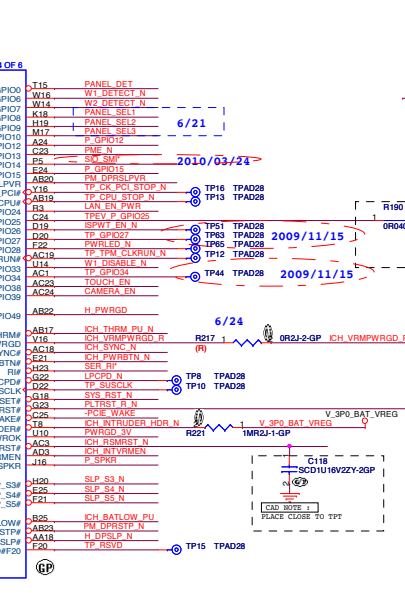
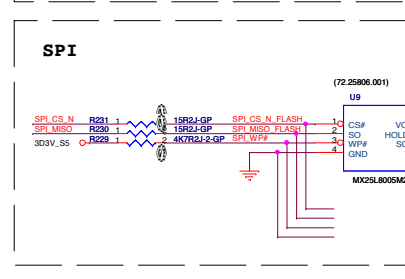
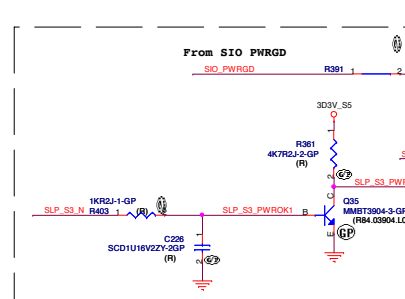
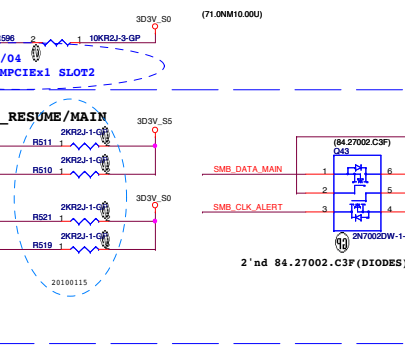
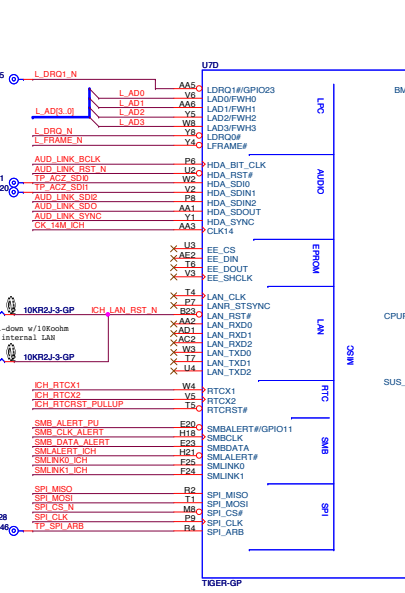
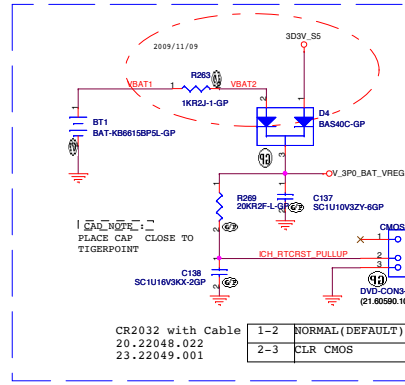
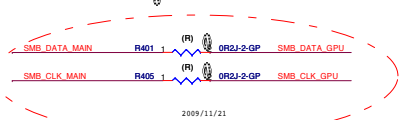
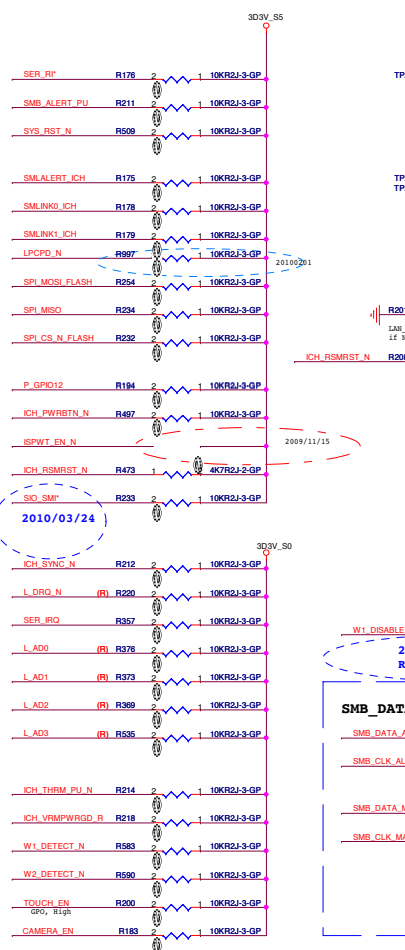
Pull- high on Page 13.

PU

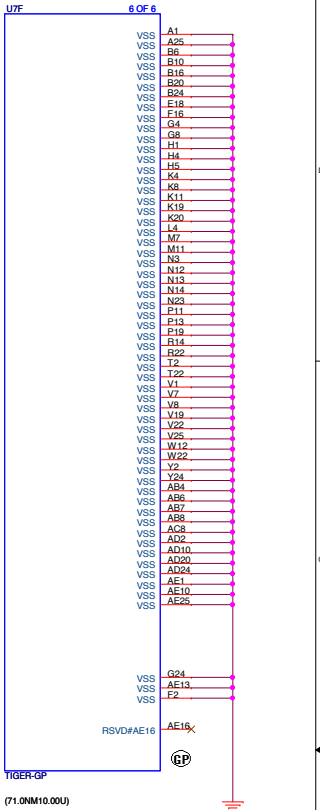
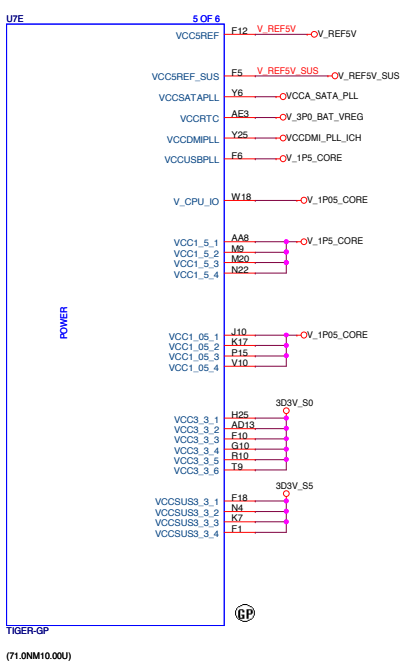
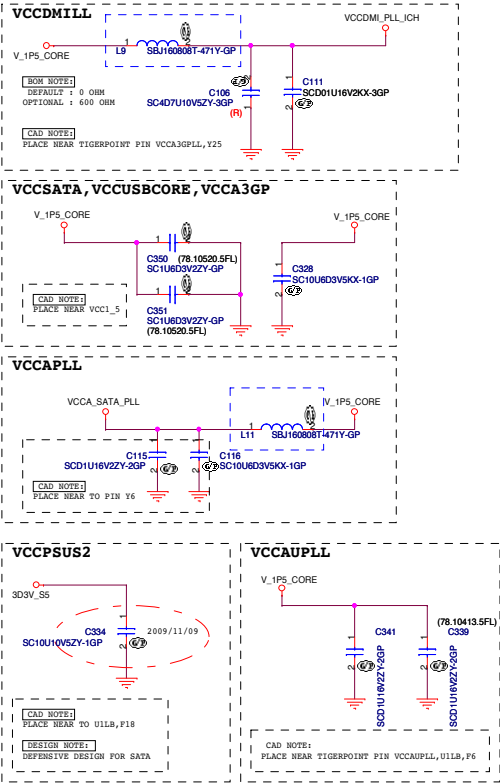
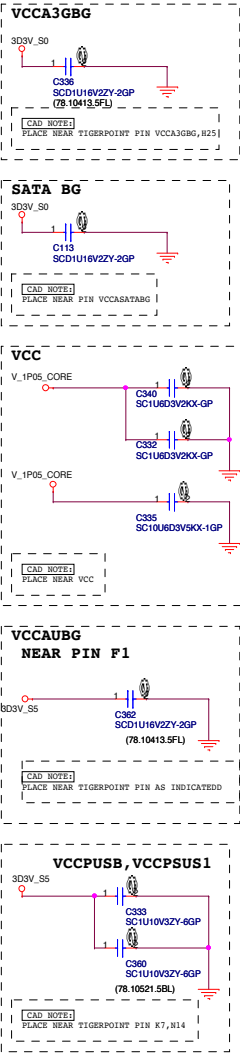
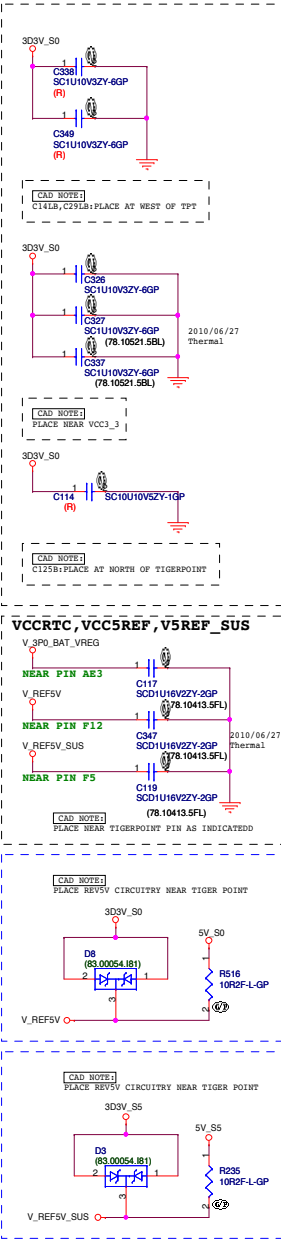


OM

MI#



MISC DECOUPLING



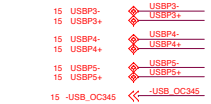
USB Port 0,6,7



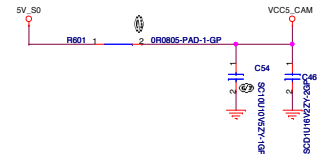
USB Port 1,2



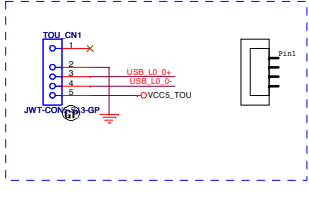
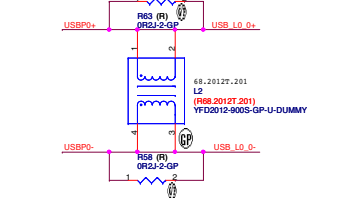
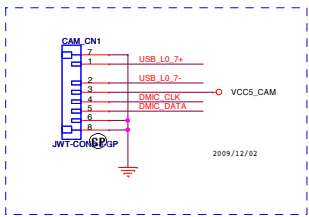
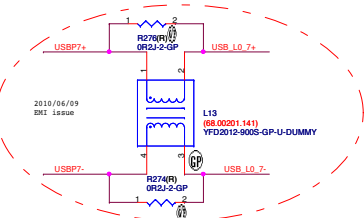
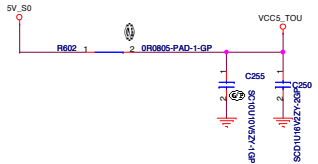
USB Port 3,4,5



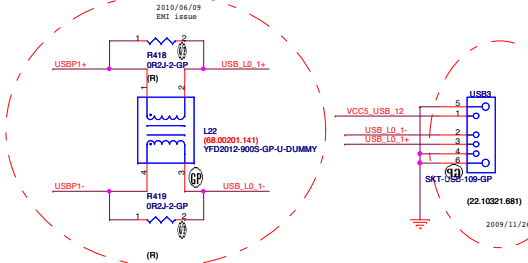
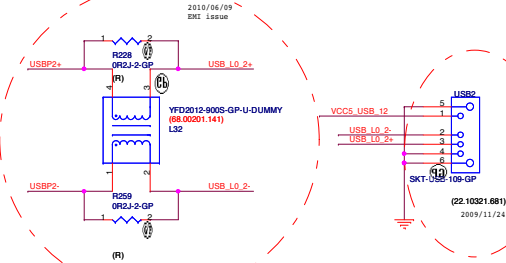
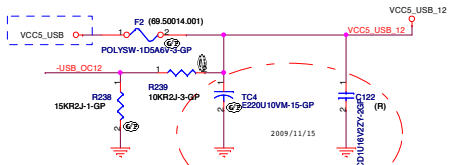
USB Port 7 -> WEB CAM



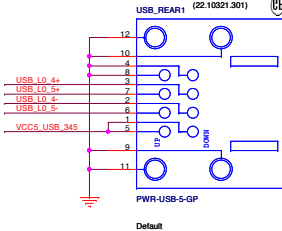
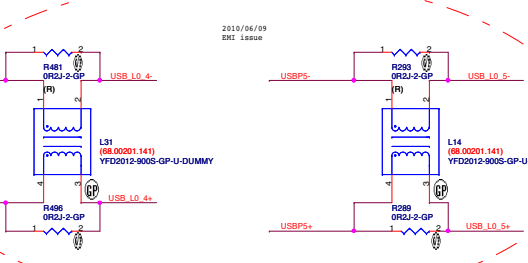
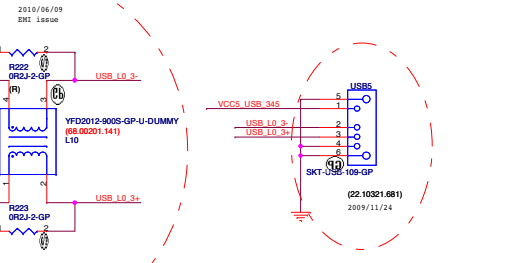
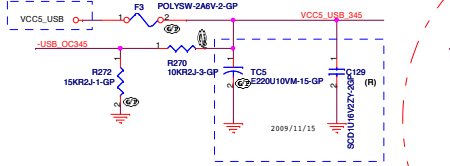
USB Port 0 -> TOUCH PANEL



USB Port 1,2 -> SIDE I/O

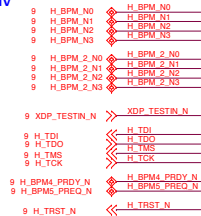


USB Port 3,4,5 -> REAR I/O



CLOCK

PNV



MISC



SATA



GULE LOGIC



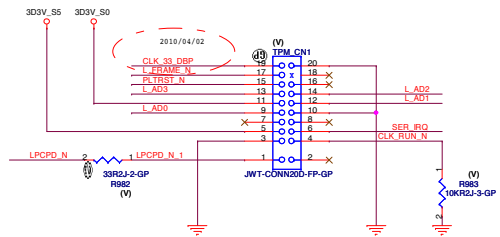
CLOCK



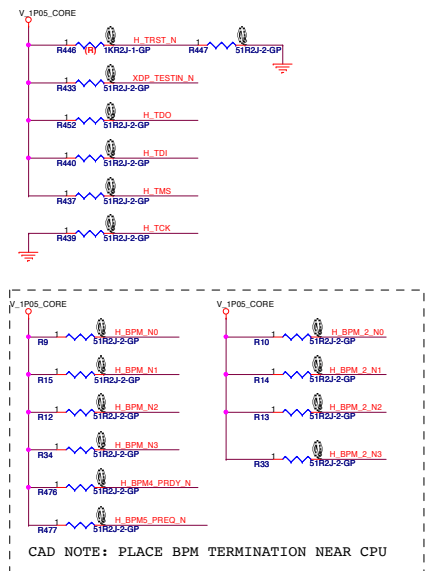
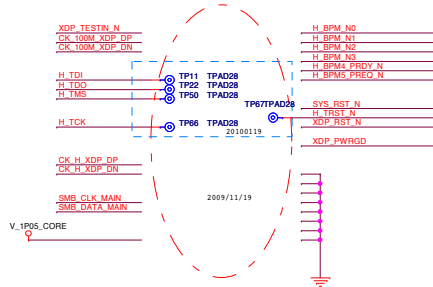
LPC



TPM Header (v MARR)

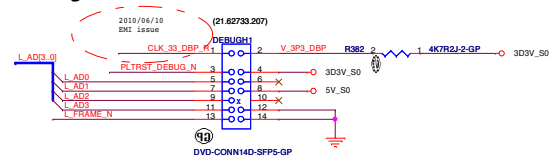


XDP-SSA
20.F1255.031

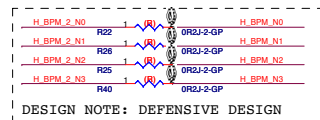


CAD NOTE: PLACE BPM TERMINATION NEAR CPU

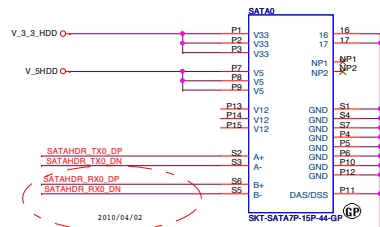
Debug Port



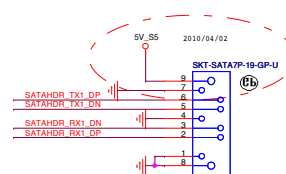
XDP CORE#2 Debug Port



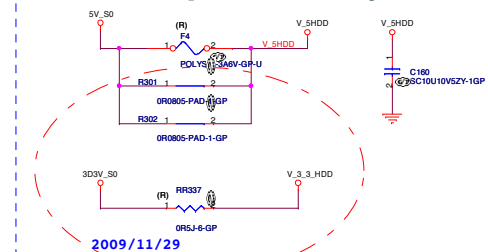
SATA0 for HDD



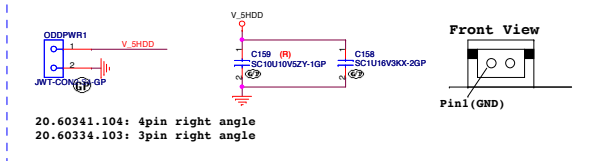
SATA1 for ODD



Layout: Put them together



2009/11/10 ODD SATA POWER CONNECTOR

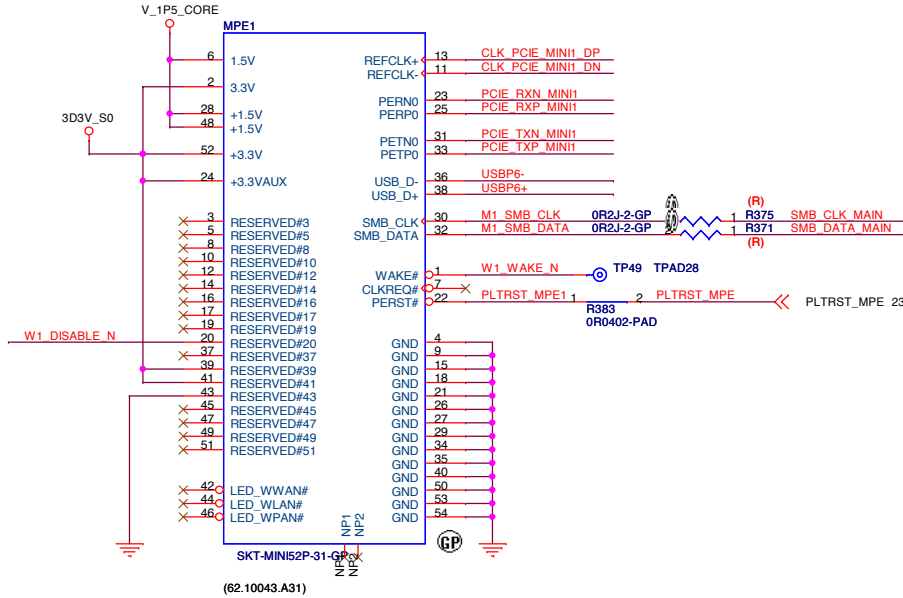


Height: 8mm
T-CONN: 62.10043.A31
TYCO: 62.10043.511

SMB

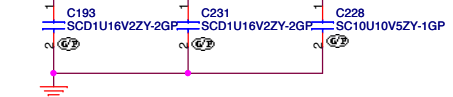


Mini PCIE Slot 1



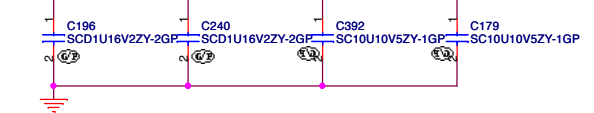
V_1P5_CORE

Please close to MPE1.



3D3V_S0

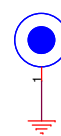
Please close to MPE1.



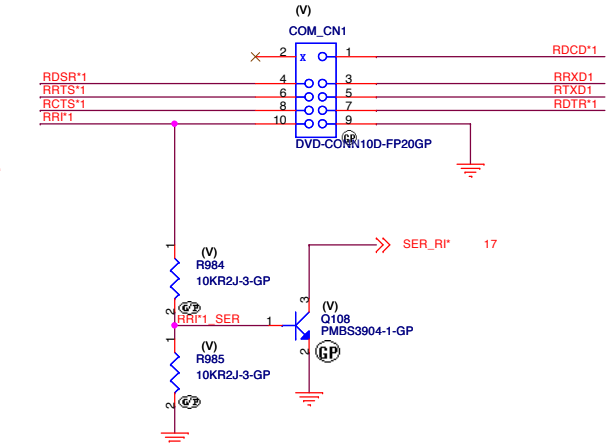
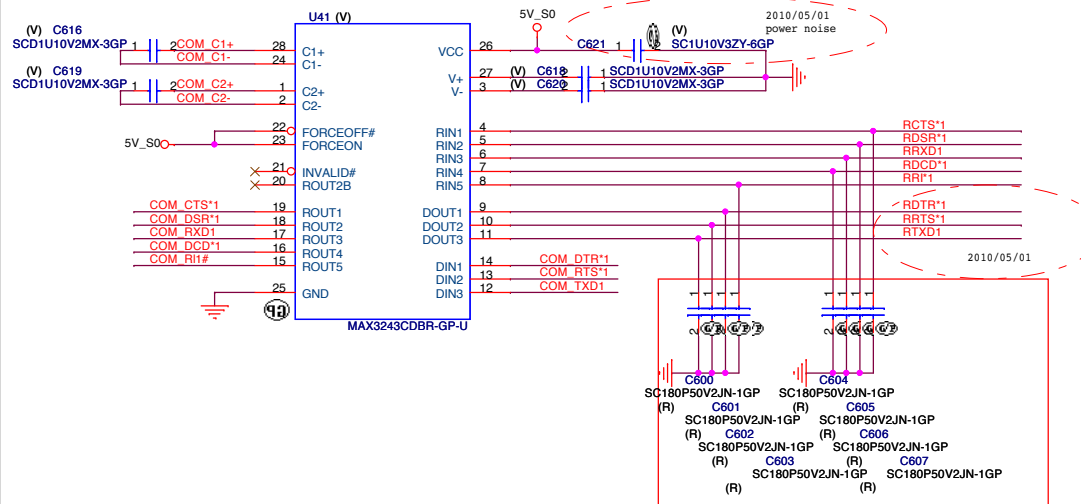
Mini PCIE holder STAND
87.61493.235 -> 5.5mm
87.00A52.220 -> 3.3mm

H3 HOLE236R102
(87.61493.235)

H4 HOLE236R102
(87.61493.235)



SERIAL PORT



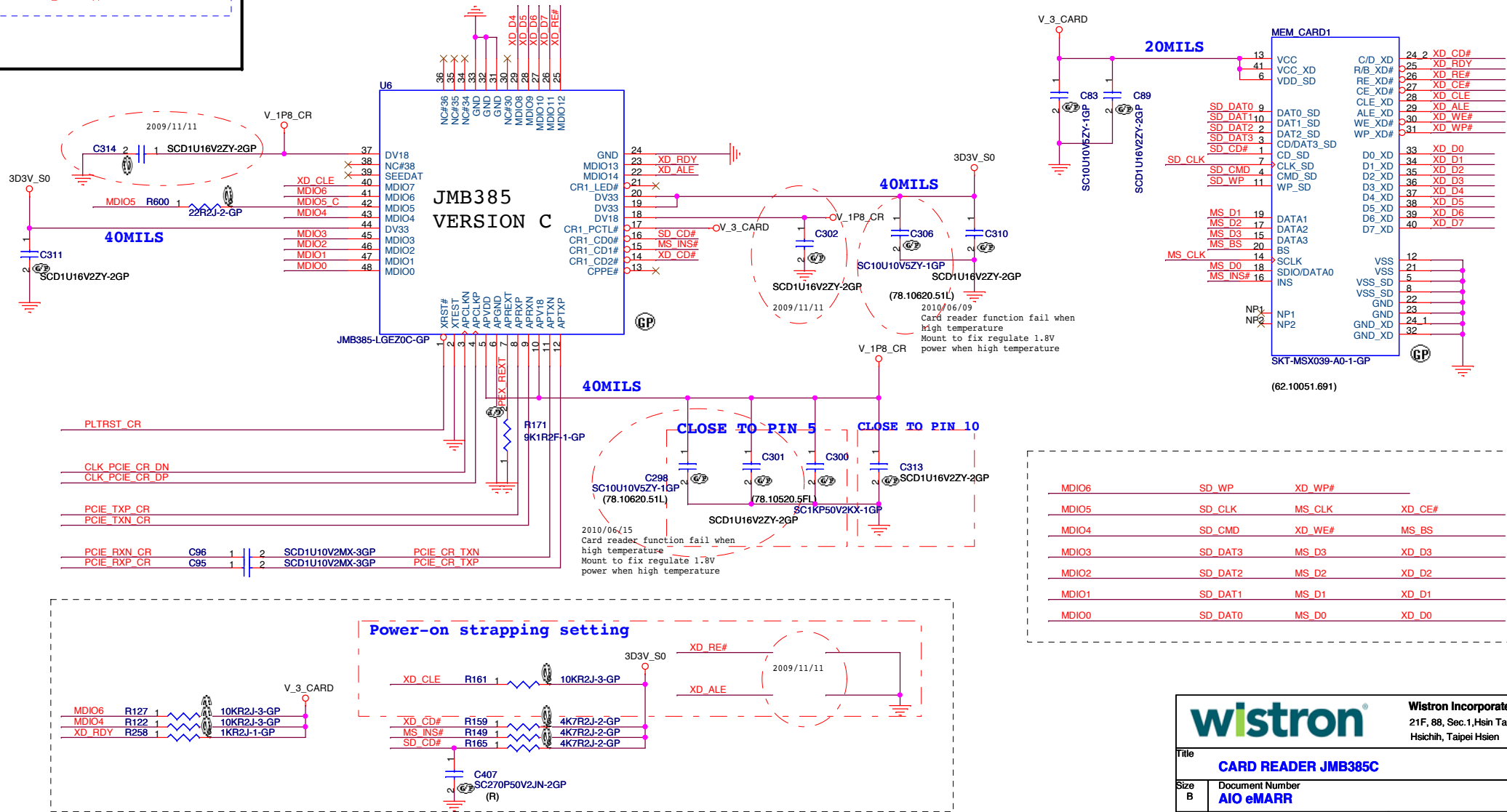
wistron

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Heiluh, Taipei Hsien

Title MINI-PCIE SLOT/COM PORT		
Size A3	Document Number AIO eMARR	Rev 1A
Date: Thursday, June 24, 2010	Sheet 24	of 31

6 CLK_PCIE_CR_DP	↔	CLK_PCIE_CR_DP
6 CLK_PCIE_CR_DN	↔	CLK_PCIE_CR_DN
15 PCIE_RXP_CR	↔	PCIE_RXP_CR
15 PCIE_RXN_CR	↔	PCIE_RXN_CR
15 PCIE_TXP_CR	↔	PCIE_TXP_CR
15 PCIE_TXN_CR	↔	PCIE_TXN_CR

23 PLTRST_CR >> PLTRST_CR

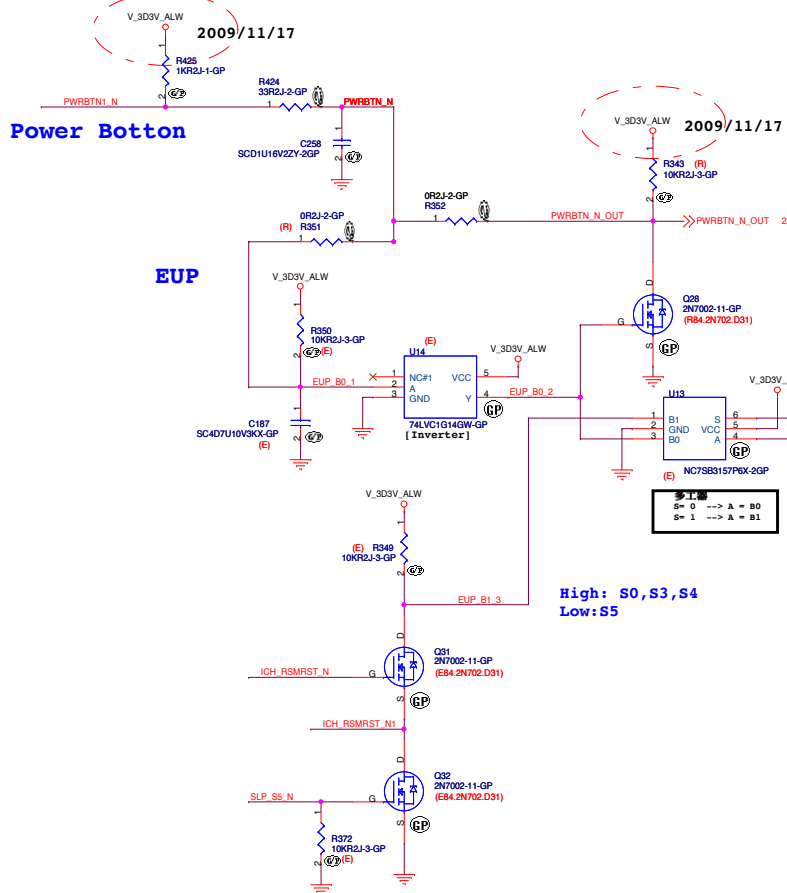
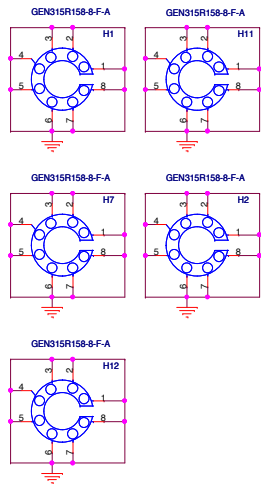


17.23 ICH_RSMRST_N >> ICH_RSMRST_N
17 SLP_SS_N >> SLP_SS_N
23 PWRBTN_N_OUT << PWRBTN_N_OUT
28 3V_5V_EN << 3V_5V_EN

Power Button

EUP

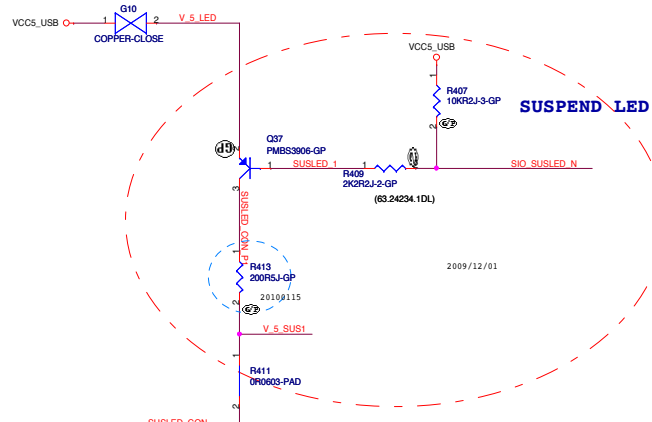
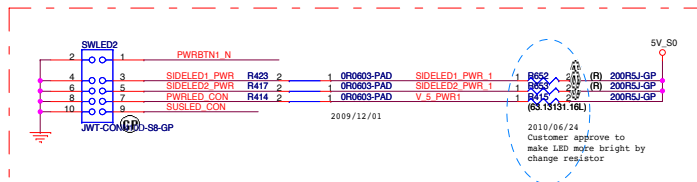
PCB MOUNTING HOLES



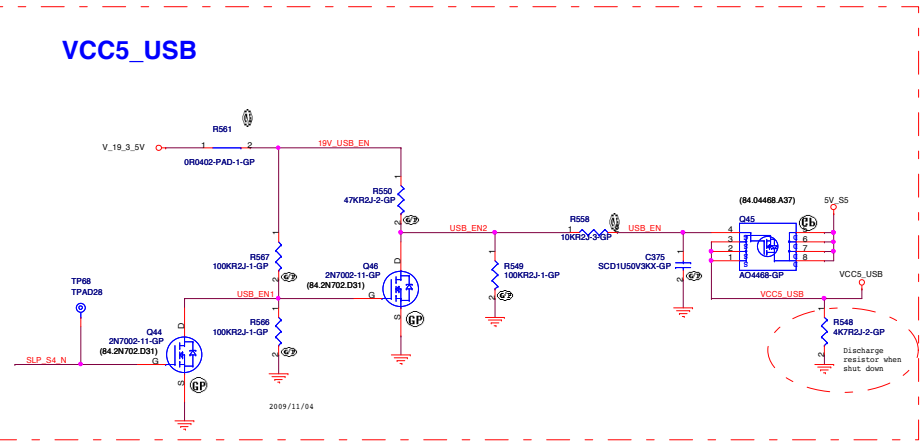
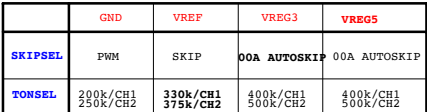
	S	R		
G3->S0	L->H	H	2-3: AC In ON	Mount R355
G3->S5->S0	H	L->H	1-2: AC In OFF	Mount R356

High: S0,S3,S4
Low:S5

	B0	B1	A	3V_5V_EN
S5	L	H	L(B0)	L
S5->S0		H->L	H(B0->B1)	L->H
S0	L	L	L(B1)	H
S0->S5	X	L->H	H(B1->B0)	H->L
S0->S4	X	L	H	H



27	3V_5V_EN	>>	3V_5V_EN
17,23,29,30	SLP_S3_N	>>	SLP_S3_N
8,17,23,29	SLP_S4_N	>>	SLP_S4_N

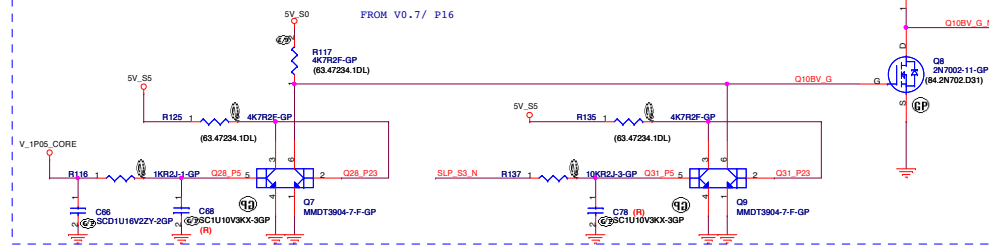
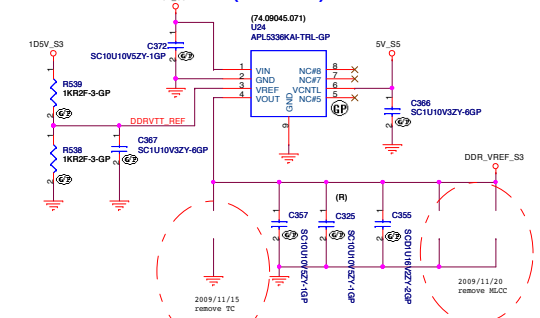


SIO

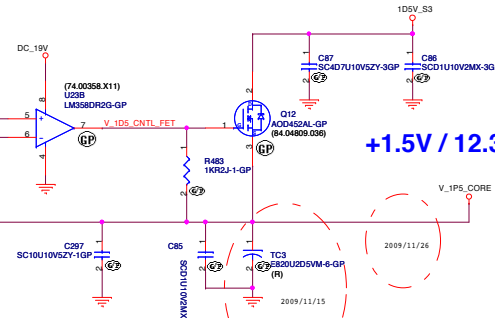
8,17,23,28 SLP_S4_N >> SLP_S4_N
17,23,28,30 SLP_S3_N >> SLP_S3_N

8 8209A_PG00D << 8209A_PG00D

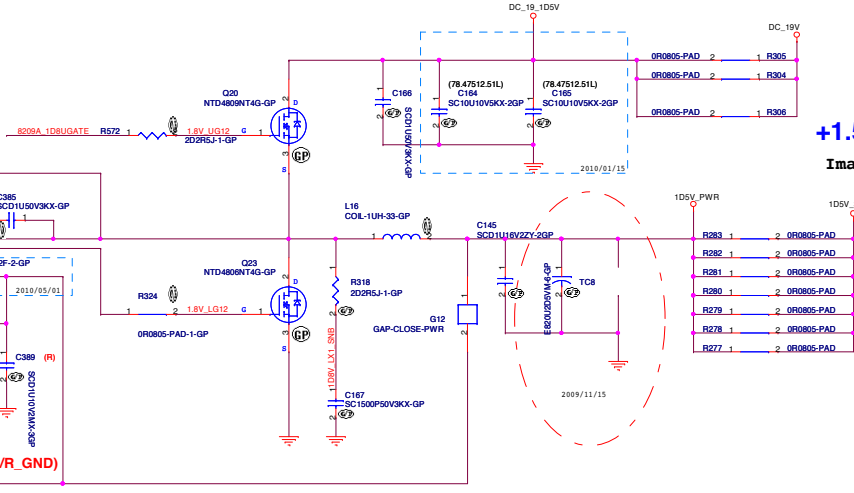
DDR2 MEM_VTT (0.75V/1A)



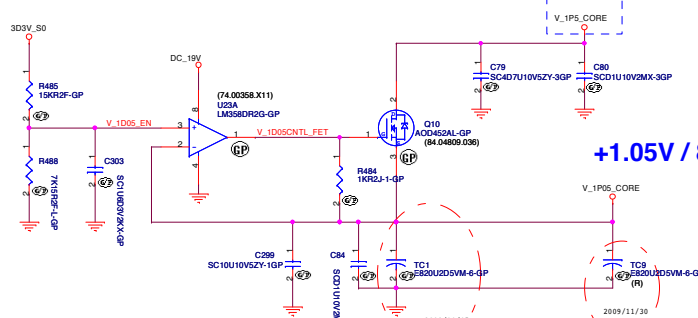
+1.5V / 12.35A



+1.5V_S3
Imax=18A



+1.05V / 8.3A



$$V_{out} = 5 \times R2 / (R1 + R2)$$

